

IIoT Solutions – WISE-2200-M

Payload Format

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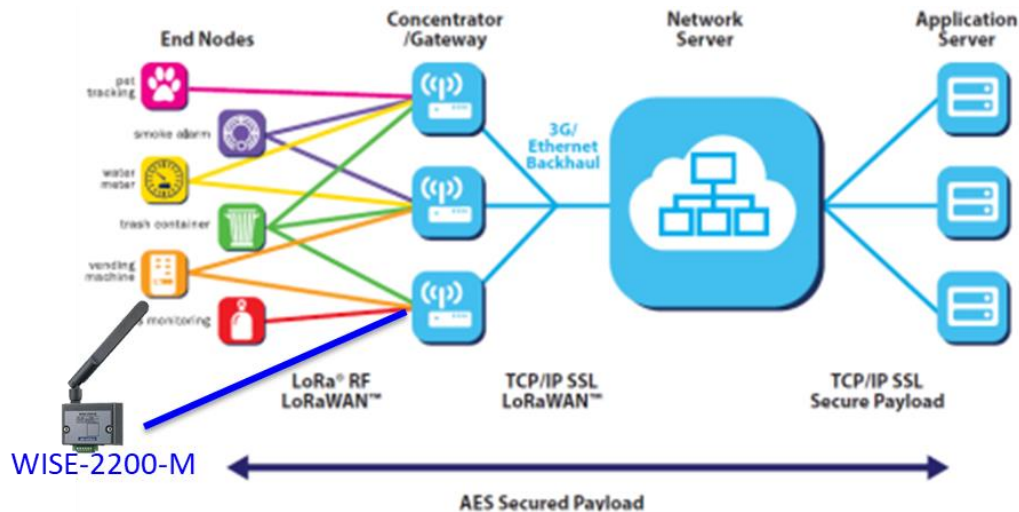
Table of Contents

Table of Contents	2
WISE LPWAN Products.....	3
1.1 LoRaWAN.....	3
2 LoRaWAN - Frame Payload.....	4
2.1 WHDR Header.....	4
2.2 WPayload.....	5
2.3 WCRC.....	5
3 WISE LPWAN Payload Format.....	6
3.1 RS-485 Coil data (I/O Type: 0x7).....	7
3.2 RS-485 Register data (I/O Type: 0x8).....	9
4 Packet Fragmentation and Reassembly	10
5 Downlink LPWAN Payload Format (Gateway to Node).....	13
5.1 Device data (I/O Type: 0x6).....	13
5.2 RS-485 Coil data (I/O Type: 0x7).....	15
5.3 RS-485 Register data (I/O Type: 0x8).....	17

WISE LPWAN Products

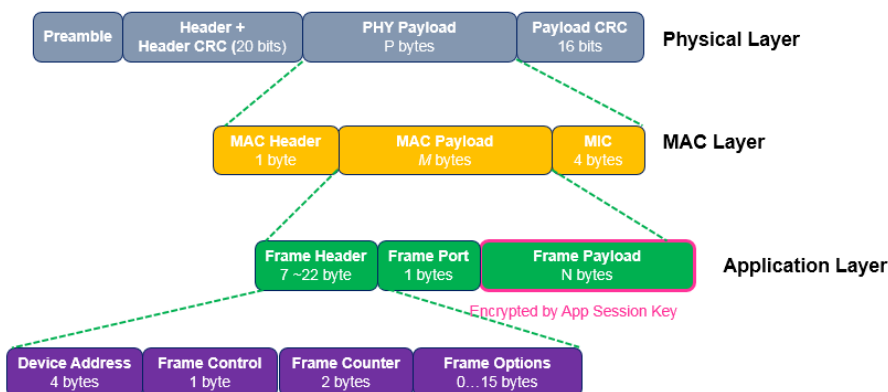
1.1 LoRaWAN

WISE-4610 series LoRaWAN nodes.



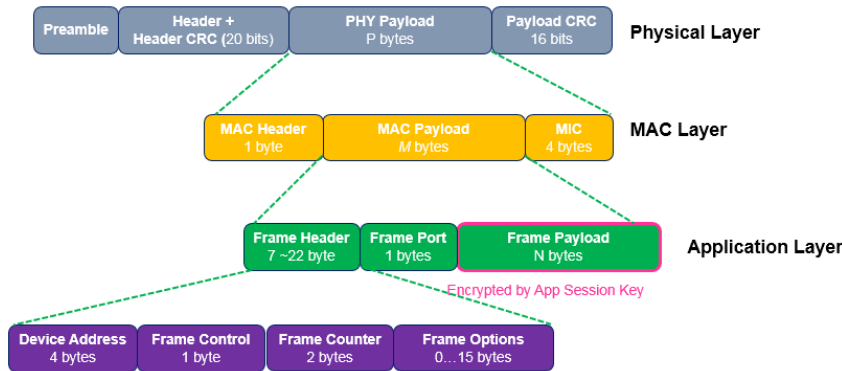
This specification describes the format of LoRaWAN Frame Payload.

LoRa Frame Format



LoRaWAN - Frame Payload

LoRa Frame Format



The message structure of LoRaWAN Frame Payload is detailed in this chapter. Each frame payload starting with a several-octets WISE data header (**WHDR**), followed by a WISE LPWAN Payload (**WPayload**), and ending with a single-octet cyclic redundancy check (**CRC**) code. A WISE Payload (WPayload) contains I/O statuses, Device information, and so on.

Frame Payload (FRM Payload)					
Octet: 1	1	0/1	0/2/8	Variable	1
Frame Control	Frame Sequence Number	Total Length	Source Address	WISE LPWAN Payload	CRC
WHDR				WPayload	WCRC

1.2 WHDR Header

Frame Control: 1 octet

Frame Control					
bit 7	6	5	4	3, 2	1, 0
First Segment				Address Mode	Frame Version
0: not first one 1: first seg.	0 Reserved	0 Reserved	0 Reserved	00: No source address 01: the least LSB 2 octets of DevEUI 10 : 8 octets DevEUI	00 : initial version 01 : 2 nd version

- First Segment bit

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Set the First Segment bit to inform the server that this is the beginning of a packet with Total Length information of WISE payload data.

- **Address Mode** 2-bits

When the Address Mode bit is unset 00, it indicates no Source Address is encapsulated. If set 01 and 10, the Source Address is the least significant two bytes and eight bytes of DevEUI, respectively.

- **Frame Version** bit

Two bits for frame structure version.

Frame Sequence Number: 1 octet, 0 ~ 255

The sequence number of data frame sent uplink to the gateway. Each time an uplink packet transmitted done, the sequence number is increased for the next new uplink.

Total Length: 1 octet (optional)

When the First Segment bit of Frame Control is set, the Total Length octet will be added to signal the server the total bytes of WISE payload data.

Source Address: 0/2/8 octets (optional)

None, 2 LSB or 8 bytes of DevEUI according to the Address Mode bit of Frame Control.

If DevEUI is 74FE48FFFF19D121, the sequential order of 2-bytes address starts with D1 21. For complete DevEUI address, the sequence will be 74 FE 48 FF FF 19 D1 21.

1.3 WPayload

The WPayload structure is detailed [chapter 4](#).

1.4 WCRC

CRC: 1 octet

An 8-bit CRC-8-CCITT value calculated from WISE Payload data. It's a standard CRC-8, with polynomial x^8+x^2+x+1 and initial value 0xFF.

Frame Version	CRC
00	CRC-8
01	~CRC-8

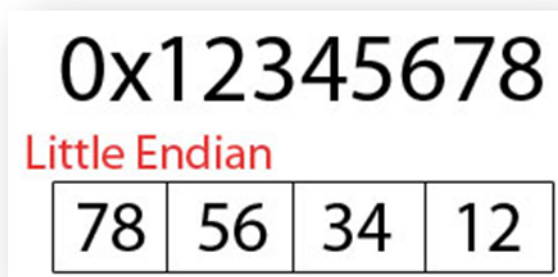
WISE LPWAN Payload Format

The message structure of WISE LPWAN Payload is detailed in this chapter. Each frame payload may contain several channels of I/O statuses and device information. Each I/O type has various data format.

For example, if there are DI 0, DI 2, AI 0, Coil 3, Coil 4, Register 1 and timestamp data to upload, the payload will contain the following segments with various length values.

WISE LPWAN Payload						
Octet: N _{DI}	N _{DI}	N _{AI}	N _{coil}	N _{coil}	N _{reg}	N _{Dev}
DI_0 Data	DI_2 Data	AI_0 Data	Coil_3 Data	Coil_4 Data	Register_ 1 Data	Timestamp

The endianness in WISE LPWAN Payload is Little-endian, the least significant bytes first.



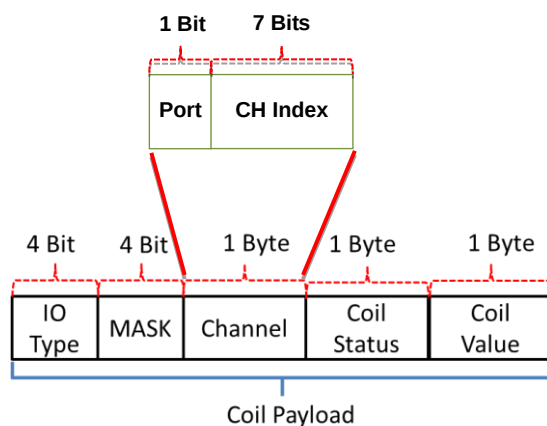
The I/O Type in each segment is used to identify the I/O or device information message type.

(4 Bit)	Message Type
0x0	DI
0x3	AI
0x5	Sensor
0x6	Device
0x7	Coil
0x8	Register

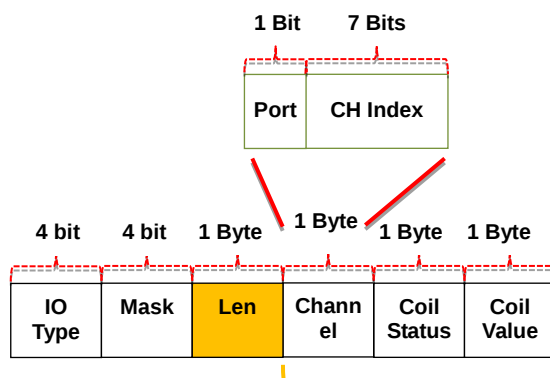
The details of I/O and device message structures are described below.

1.5 RS-485 Coil data (I/O Type: 0x7)

1.5.1 Sub-1G and LoRaWAN ver.00



1.5.2 LoRaWAN ver.01



- **Len** (1 octet): 1 ~ 255
number of bytes after this octet (**Len**)

- **IO Type** (bit 7 – 4): 0x7

- **MASK** (bit 3 – 0)

Bit 0	Coil Status
Bit 1	Coil Value

- **Channel** (1 octet):

COM port number and coil channel index.

Bit 0 ~ 6	Coil Channel Index: 0 ~ 127
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Bit 7	COM Port Index: 0 – COM port 1
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■ Coil status: 1 octet

The error status of polling this coil

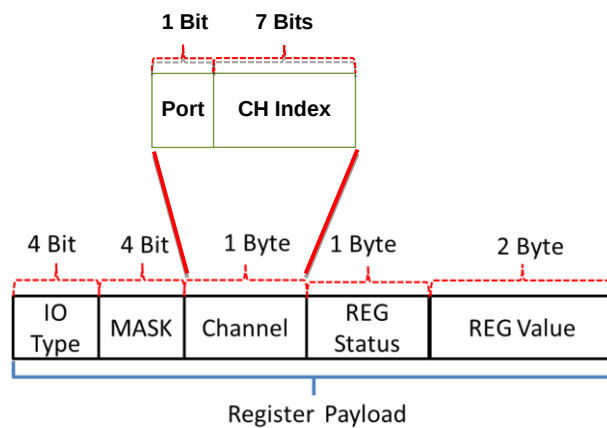
Status Value	Description
0 (0x00)	No error
1 (0x01)	Illegal function
2 (0x02)	Illegal data address
3 (0x03)	Illegal data value
4 (0x04)	Slave device failure
5 (0x05)	Acknowledge
6 (0x06)	Slave device busy
7 (0x07)	Negative acknowledge
8 (0x08)	Memory parity error
9 (0x09)	Reserved
10 (0x0A)	Gateway path unavailable
11 (0x0B)	Gateway target device failed to respond
12 ~15	Reserved
16 (0x10)	Unavailable
17 (0x11)	Slave response timeout
18 (0x12)	Checksum error
19 (0x13)	Received data error
20 (0x14)	Send request fail
21(0x15)	Unprocessed
22(0x16)	Read only
23(0x17)	In processing

■ Coil value: 1 octet

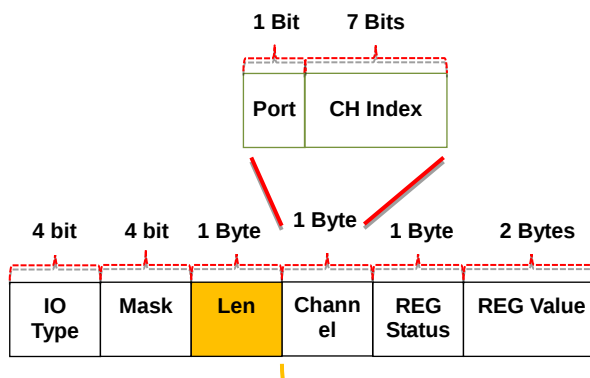
The coil data, 0 or 1

1.6 RS-485 Register data (I/O Type: 0x8)

1.6.1 Sub-1G and LoRaWAN ver.00



1.6.2 LoRaWAN ver.01



- **Len** (1 octet): 1 ~ 255
number of bytes after this octet (**Len**)

- IO Type (bit 7 – 4): 0x8

- MASK (bit 3 – 0)

Bit 0	Register Status
Bit 1	Register Value

- Channel (1 octet):

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COM port number and register channel index.

Bit 0 ~ 6	Register Channel Index: 0 ~127
Bit 7	COM Port Index: 0 – COM port 1

■ Register status: 1 octet

The error status of polling this channel can refer to Coil Status in the previous section.

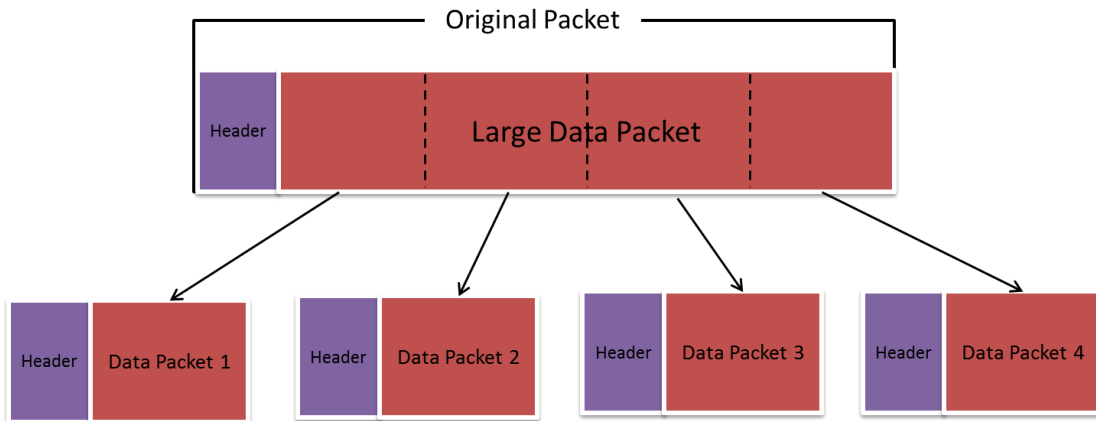
■ REG value: 2 octets

The register data with range 0 to 0xFFFF

2 Packet Fragmentation and Reassembly

Because the data rate is controlled by the network, the length of each uplink is not fixed. The Frame Payload (FRM Payload) will be split into multiple fragments.

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A complete frame can be divided into several uplink messages.

Frame Payload (FRM Payload)		
WHDR	WPayload	WCRC

1st message:

WHDR				WPayload*
Octet: 1	1	1	0	Variable
Frame Control	Frame Sequence Number	Total Length	Source Address	A partial of WISE Payload
0x80	S	M		

2nd ~ nth messages

WHDR				WPayload*
Octet: 1	1	0	0	Variable
Frame Control	Frame Sequence Number	Total Length	Source Address	A partial of WISE Payload
0x00	(S+1) ~			

The last message:

WHDR				WPayload*	WCRC
Octet: 1	1	0	0	Variable	1
Frame Control	Frame Sequence	Total Length	Source Address	The rest of WISE Payload	CRC

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D-01-F10 Rev.A1

	Number				
0x00	(S+n)				0x23

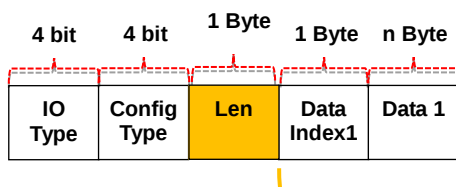
3 Downlink LPWAN Payload Format (Gateway to Node)

The LoRaWAN frame version in WHDR header is **ver.00**.

FPort for data downlink is identical to uplink FPort.

3.1 Device data (I/O Type: 0x6)

***Single index per frame only**



■ IO Type (bit 7 – 4): **0x6**

■ Config Type (bit 3 – 0):

0	Reserved
1	General configurations
2	LPWAN application configurations
3	
4	

■ Len (1 octet): 1 ~ 255

Total data length of all indexes and its data

■ Data Index: 1 octet

■ Data: n octets

3.1.1 General (Type: 0x61)

Data index	Data length n	Data content
1	4	Adjust RTC time by UNIX timestamp of UTC time (4 bytes).
2	~25 + 1 Where 1 octet is 0x00 (NULL end)	Adjust RTC time by ISO 8601 format YYYY-MM-DDThh:mm:ssTZD where: YYYY = four-digit year MM = two-digit month (01=January, etc.) DD = two-digit day of month (01 through 31) hh = two digits of hour (00 through 23) (am/pm NOT allowed) mm = two digits of minute (00 through 59) ss = two digits of second (00 through 59) TZD = time zone designator (Z or +hh:mm or -hh:mm)
3	3	Restart the system Write: RST
4	4	Adjust RTC time by an offset value in unit of seconds. Value range: -2,147,483,647 ~ +2,147,483,647 (signed 4-byte)

[Example]:

To set the RTC time to 2019-12-26T10:55:30+08:00

[0x80, seq, 0x1D,]0x61, 0x1B, 0x02, '2', '0', '1', '9', '-', '1', '2', '-', '2', '6', 'T', '1', '0', ':', '5', '5', ':', '3', '0', '+', '0', '8', ':', '0', '0', 0x00, [CRC]

To restart the module

[0x80, seq, 0x06,]0x61, 0x04, 0x03, 'R', 'S', 'T', [CRC]

To adjust the RTC time by offset -120 seconds

[0x80, 0x01, 0x07,] 0x61, 0x05, 0x04, 0x88, 0xFF, 0xFF, 0xFF, 0xF3

To adjust the RTC time by offset +120 seconds

[0x80, 0x01, 0x07,] 0x61, 0x05, 0x04, 0x78, 0x00, 0x00, 0x00, 0xFF

3.1.2 LPWAN Application (Type: 0x62)

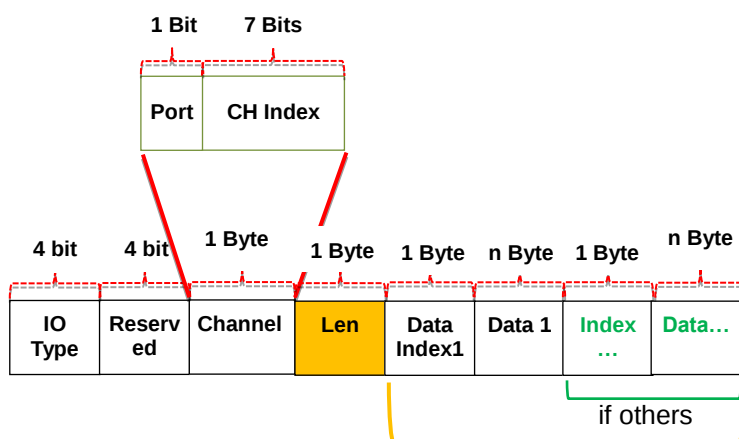
Data index	Data length n	Data content
1	4	The interval of updating I/O data. Value range: 1 ~ 2592000 seconds
2		
3		
4		

[Example]:

To set the Data updating interval to 15 seconds (Little Endian)

[0x80, seq, 0x07,]0x62, 0x05, 0x01, 0x0F, 0x00, 0x00, 0x00, [CRC]

3.2 RS-485 Coil data (I/O Type: 0x7)



■ IO Type (bit 7 – 4): 0x7

■ Channel (1 octet):

COM port number and coil channel index.

Bit 0 ~ 6	Coil Channel Index:
-----------	---------------------

	0 ~ 127
Bit 7	COM Port Index: 0 – COM port 1

■ Len (1 octet): 1 ~ 255

Total data length of all indexes and its data

■ Data Index: 1 octet

■ Data: n octets

Data index	Data length n	Data content
1	1	Set Coil Value Write 0 or 1
2		Reserved
0x80	8	Configure the Scan Interval value (seconds) of certain rules. Rule index mask (4) + Scan Interval (4)

[Example]:

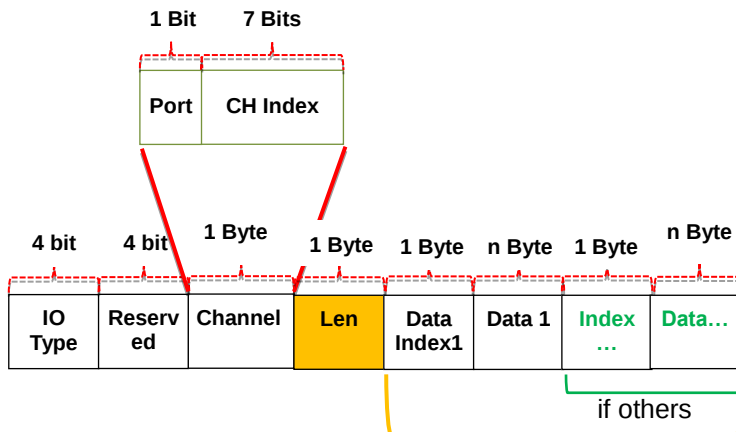
To set the coil channel 4 of COM port 2 to 1

[0x80, seq, 0x05,]0x70, 0x84, 0x02, 0x01, 0x01, [CRC]

To set the Scan Interval value of rule index 0 and 9 of COM port 2 to 300 (0x12C) seconds.

[0x80, seq, 0x0C,]0x70, 0x80, 0x09, 0x80, 0x01, 0x02, 0x00, 0x00, 0x2C, 0x01, 0x00, 0x00, [CRC]

3.3 RS-485 Register data (I/O Type: 0x8)



■ IO Type (bit 7 – 4): 0x8

■ Reserved (bit 3 – 0): 0x0

■ Channel (1 octet):

COM port number and Register channel index.

Bit 0 ~ 6	Register Channel Index: 0 ~ 127
Bit 7	COM Port Index: 0 – COM port 1

■ Len (1 octet): 1 ~ 255

Total data length of all indexes and its data

■ Data Index: 1 octet

■ Data: n octets

Data index	Data length n	Data content
1	2	Set Register Value Write 0 ~ 0xFFFF
2		Reserved
0x80	8	Configure the Scan Interval value (seconds) of certain rules. Rule index mask (4) + Scan Interval (4)

[Example]:

To set the Register channel 31 of COM port 1 to 0x3184

[0x80, seq, 0x06,]0x80, 0x1F, 0x03, 0x01, 0x84, 0x31, [CRC]

To set the Scan Interval value of rule index 0 and 9 of COM port 2 to 300 (0x12C) seconds.

[0x80, seq, 0x0C,]0x80, 0x80, 0x09, 0x80, 0x01, 0x02, 0x00, 0x00, 0x2C, 0x01, 0x00, 0x00, [CRC]